



**SUPPLEMENTAL  
INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

ATTY. DOCKET NO.  
10746/32

U.S. SERIAL NO.  
10/092,089

APPLICANT  
Keiji KISHINE et al.

FILING DATE  
March 5, 2002

GROUP  
2859

**U. S. PATENT DOCUMENTS**

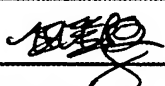
EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
LW	6,259,755	July 10, 2001	Eugene O'Sullivan et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
LW	5-56410	March 5, 1993	Japan			Abst.	

**OTHER DOCUMENTS**

EXAMINER INITIAL		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
LW		M. Wurzer et al., "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz Silicon Bipolar Technology," IEEE J. Solid-State Circuits, Vol. 34, No. 9, pp.1320-1324 Sep. 1999.

EXAMINER		DATE CONSIDERED	10/3/05
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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PTO-1449 FORM

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
LW	06252654	September 9, 1994	Japan			X	
LW	11055082	February 26, 1999	Japan			X	
LW	10126400	May 15, 1998	Japan			X	

\* Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by International Searching Authority).

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OTHER DOCUMENTS

EXAMINER INITIAL	Technology Center 2600	
	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	
LW	Noboru Ishihara, Yukio Akazawa, "A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit Using the Sample-and-Hold Technique", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 29, NO. 12, DECEMBER 1994, pp. 1566-1571.	
LW	D. Clawin, U. Langmann, "Multigigabit/second Silicon Decision Circuit", ISSCC 85, February 1985, pp.222-223.	
LW	M. Wurzer, J. Bock, W. Zirwas, H. Knapp, F. Schumann, A. Felder, L. Treitinger, "40Gb/s Integrated Clock and Data Recovery Circuit in a Silicon Bipolar Technology", IEEE BCTM 8.1, Sep. 27-29, 1998.	
LW	J. Savoj, B. Razavi, "A 10 Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection", ISSCC 2001, February 5, 2001.	
LW	D. Clawin, U. Langmann, B.G. Bosch, "Silicon Bipolar Decision Circuit Handling Bit Rates up to 5Gbit/s", Journal of lightwave technology, Vol. LT-5, No. 3, March 1987, pp.348-354.	

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